Amendments to the Specification

Replace page 3, line 23, through page 5, line 18, as follows:

Fig. 2 shows the phase locked loop 4 in ~~an~~ a data receiver 2 including a phase detector PD 6, a loop filter LF 8 and an analogue voltage controlled oscillator VCO 10. The incoming data flow 12 is indicated at "data in". The output 14 of the voltage controlled oscillator VCO 10 is indicated with "clock". The circuit functions to sample the incoming data 12 with the clock frequency and to recover timing information for the voltage controlled oscillator VCO 10 to generate the correct clock 14 frequency with the correct phase for sampling the incoming signal 12.

Fig. 3 shows controlled by the clock signal 14 CLK sampling times AA, A, T, B and BB for the incoming data flow 12. Times AA, A, B and BB are in intervals of one bit, whereas time T is at signal transition between two adjacent bits at times A and B in the data flow 12. The signal samples at A, T and B form an "inner sample group" as used in a conventional early-late phase detector and the signal samples AA, A, T, B, BB form an "enlarged sample group". Samples AA and A form a first signal sample pair and samples B and BB form a second signal sample pair.

Fig. 4 shows the circuitry for correcting the phase of the clock 14 in the data receiver 2. The incoming data 12 are connected to a first shift register SR1 and a second shift register SR2. Shift register SR1 has four flip flops FF1, FF2, FF3, FF4 in a row which form stages or cells which receive the ~~sampling probes~~ samples indicated in Fig. 3 and shift them from stage to stage to ~~in~~ the timing of the clock. Shift register SR2 has three flip flops FFa, FFb, FFc in a row which form stages or cells ~~where the~~ of the row. The first cell in the row is addressed by the falling edge of the clock pulse so as to sample an expected signal transition T and ~~store it~~ intermediately store it and shift it to the output of the shift register SR2 in the same ~~a~~ time period as ~~when~~ sample probe A appears at the output of the third cell of shift register SR1.

The phase detector 6 also includes a first gate circuit GC1 and a second gate circuit GC2. Gate circuit GC1 is configured in two rows where each row comprises an (EXOR) Exclusive-or (XOR) gate 5 as input stage, an AND gate 7 having one inverted input as the second stage, a flip flop 9 as the third stage and a weighting output stage 11 which delivers a control output to be delivered to the loop filter LF 8 and hence to the voltage controlled oscillator VCO 10 for controlling same. The output signal of the upper row is termed "UP" and of the lower row "DOWN". UP means shifting the edges of the clock CLK to the left in Fig. 3 and DOWN means shifting to the right hand side. The output stages of the gate circuit GC1, each comprises a second input (SI) from gate Circuit GC2 which can switch the output stage into a condition of multiplying the output signal UP or DOWN by a scaling or amplification factor x which has a value between 1 and 4. Further circuitry (not shown) may evaluate the quality of the incoming data signal and deliver a setting signal to set the value of factor x at an appropriate level.

Gate circuit GC2 has a pair of EXNOR Exclusive-nor (XNOR) gates 13 at the input, an AND gate 15 connected to the outputs of the EXNOR XNOR gates and a flip flop 17 as output stage provided for timing purposes and being connected to the output stages of the first gate circuit GC1.

The conventional early-late phase detector of Alexander is indicated at APD 3 in Fig. 4, wherein the symbols BB and B are to be exchanged for B and A. The operation of the detector APD 3 can best be understood from table 1 wherein the signal samples are taken at times A, T and B. The signal value can be "high" indicated by 1, or "low" indicated by 0.

The signal transition at time T may have a value which is nearer to low, then the sample value is 0, or nearer to high, then the sample value is 1. There are patterns of the signal samples which produce an output for controlling the voltage controlled oscillator VCO 10, and patterns from which no information for controlling the VVO VCO 10 can be derived. (Output UP =0, DOWN=0).

Replace page 5, line 25, to page 6, line 11, as follows:

Signals carrying a data flow may show data bit patterns with a pair of 11 and a pair of 00 and a transition between such pairs. Also data bit patterns 00 followed by 11 are possible. In signal sections with such bit pairs, the transitions between the pairs may be termed "half rate transitions". These half rate transitions produce Eye openings 21,23 shown at the left hand side and right hand side of Fig. 1. Finding these half rate transitions and using them for clock control will result in a good phase correction. The novel features of the early-late phase detector of the invention lead to these excellent characteristics.

Table 2 shows signal samples at sampling times AA, A, T, B, BB, the logical equations belonging thereto and the output signal from the improved early-late phase detector. As shown, the improved detector is able to find signal patterns with pairs of signal values having the same signal levels "high" or "low". The signal transition between adjacent pairs may be high (1) or low (0). In any case, such patterns of signal samples are valuable to control the VCO 10 and therefore are stronger weighted than any other patterns. The circuitry for doing so has already been explained with Fig. 4.